**Digital System design Lab CSE-308L**

**Semester:6th**



**Lab Report # 5**

**RING COUNTERS**

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**Section: A**

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**Lab 5**

**Implementation of a 8 bit Ring Counter**

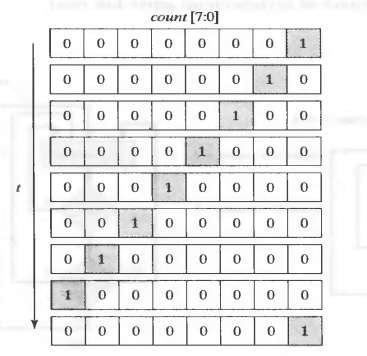
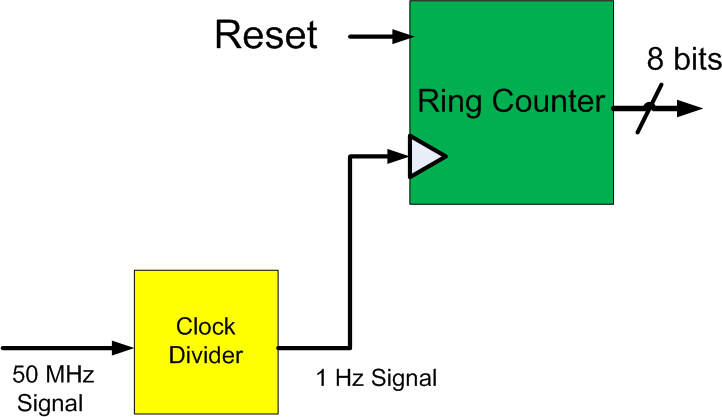
**Objective:**

* To become familiarized with behavior level modeling
* To be able to implement sequential circuits using Verilog
* To Implement an 8 Bit Ring Counter on Spartan 6 FPGA starter kit.

**Block Diagram:**

The Spartan 6 kit has a clock source of 100 MHz. If we use it in applications like counters, the counter will count at an incredibly fast speed and we will not be able to see the output. Your task is to divide the 100 MHz frequency into a 1 Hz frequency. The Module Clock divider is responsible will be responsible for it.

The functional detail of the 8-bit Ring Counter is shown in the following figures.



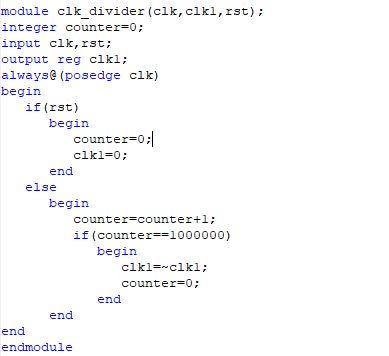
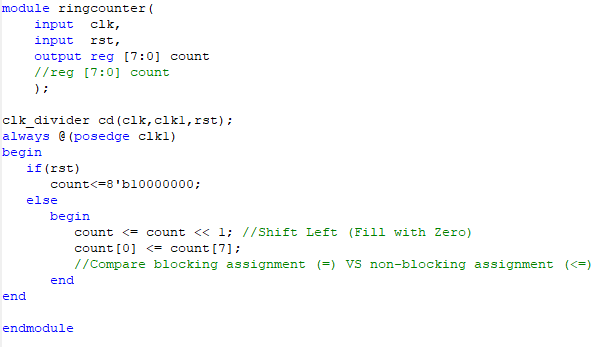
**100 MHz Signal**

Pictorial View of the Operation of a Ring Counter

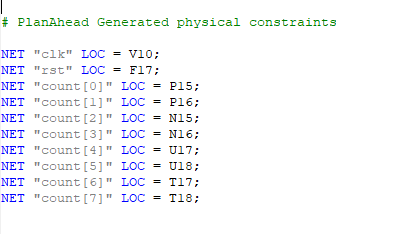
**I/O Connection:**

The output of the Ring Counter should be connected to 8 LEDs on Spartan 3 Starter Kit. The clock input is connected to pin “T9” on the board. The LEDs should turn on and off one by one from left to Right with an interval of 1 second.

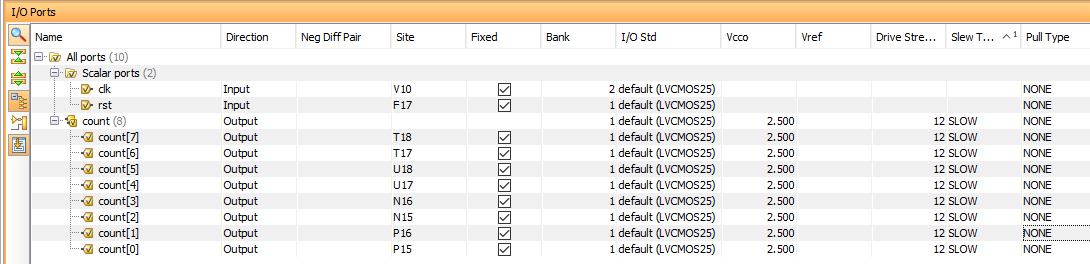
**CODE:**



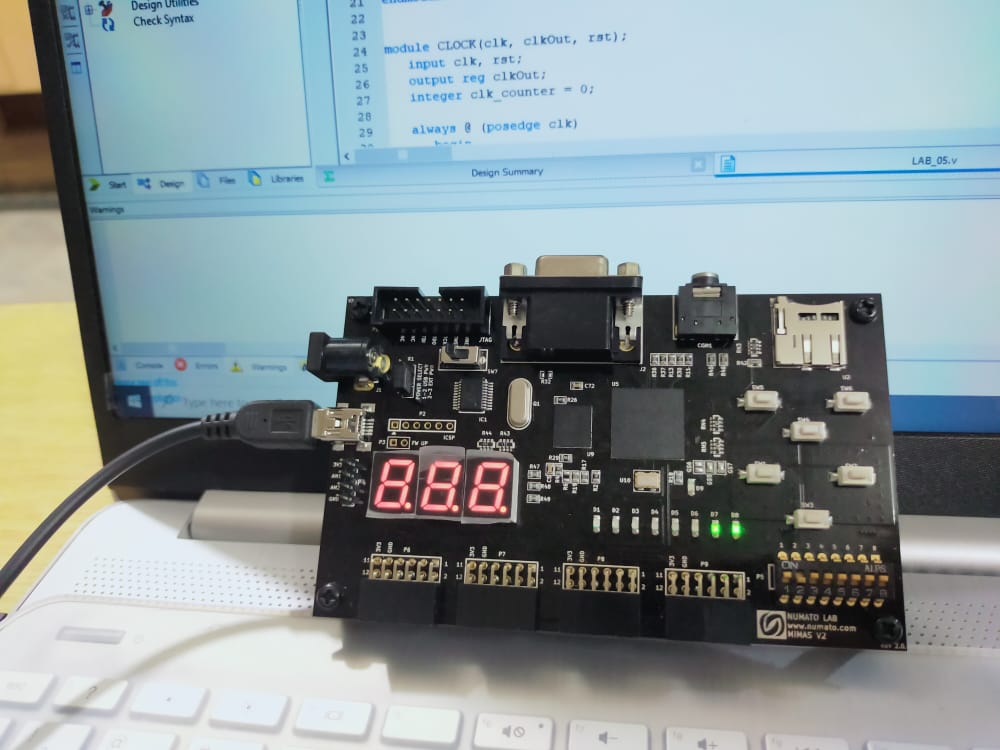
**UCF FILE:**

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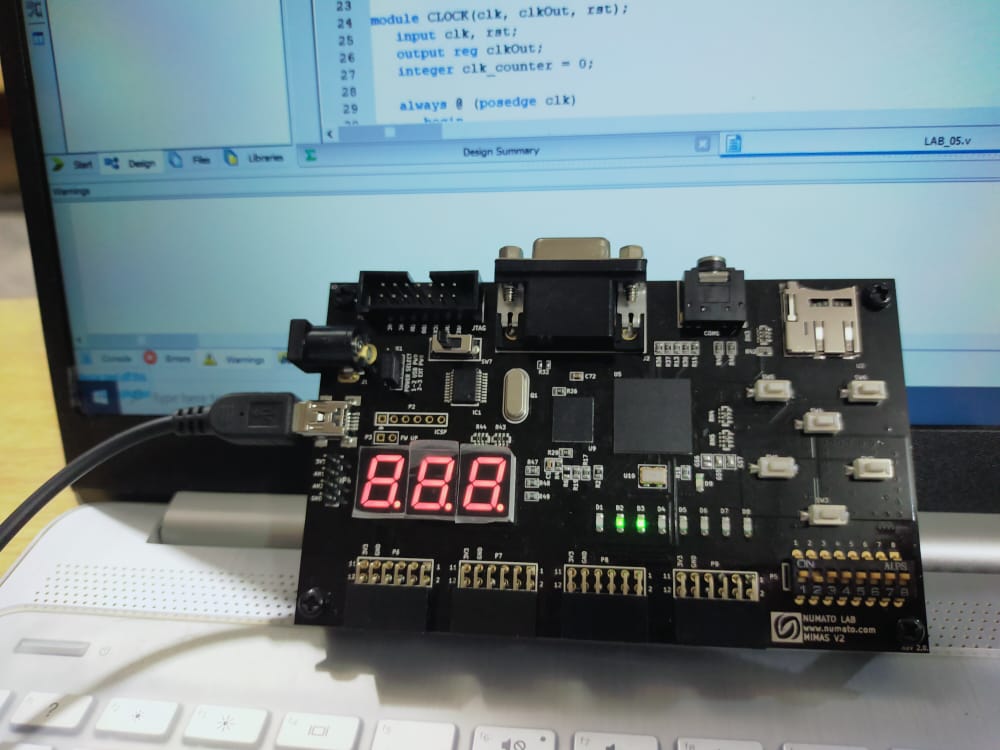
**I/O PIN PLANNING:**



**OUTPUT:**

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